Lab 1: Cadence® Custom IC design tools- Setup, Schematic capture and simulation

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Introduction

The main goal of this lab is to become familiarized with the basic functions of the Cadence® Custom IC design tool, Virtuoso®. To begin this lab, I started with setting up my account to run the IC tool. After this was completed, I learned how to manage my files with the Library Manager, recognize the basics of the Schematics Editor, and use Analog Design Environment (ADE) to simulate a simple low-pass RC circuit.

Pre-lab

The following pages include my results to the pre-lab questions.

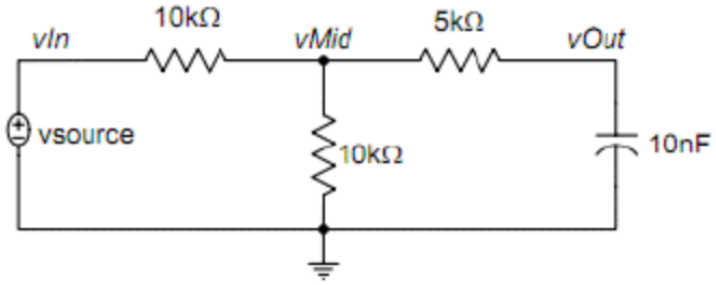

Figure 1: Pre-lab circuit

Procedure

1. Setup

After logging into the system, many steps were required to take before begin using the IC design tools:

A) Set Bash Shell for the account

Login to: http://www.asw.iastate.edu.
Click on: Manage user "Net-ID"
Click on: Set your login shell (Unix/Linux)
Select: "/bin/bash"
Click on: Update Shell
Click on: logout

B) Create a ~/.software file (Only once)

To enable the use of different software tools, CSG has made a special file.software in their home directory customized for their use. I opened the terminal and entered "gedit ~/.software" and entered the following lines in that file:

```
IC
CALIBRE
ASSURA
MMSIM
EDI
```

These five entries enable the use of the IC design tools with analog and digital design flow capability. I will use this file in the future if other tools are needed.

C) Create a ~/.bashrc file (Only once)

This file includes to following content:

```
if [ -f /etc/bashrc ]; then
. /etc/bashrc
fi
```

D) Create a ~/.bash_profile file (Only once)

I followed the following lines in that file:

```
if [ -f ~/.bashrc ]; then
. ~/.bashrc
fi
# User specific environment and startup programs
PATH=$PATH:$HOME/bin
BASH_ENV=$HOME/.bashrc
USERNAME=""
export USERNAME BASH_ENV PATH DISPLAY
```

E) Create a ~/cds.lib file (only once)

The Library Manager retains information about system-wide libraries as well as personal design libraries in a special file called cds.lib. For better organization purposes, I created a cds.lib in my home directory. This file includes definitions of system wide libraries. For starters, I created the file with the following contents:

INCLUDE /usr/local/cadence/iclocal/local/cdssetup/cds.lib

DEFINE analogLib $IC/tools/dfII/etc/cdslib/artist/analogLib

The first line includes a cds.lib file created by the system administrators from another location on the system. The second line defines a library "analogLib" supplied by Cadence, which includes most basic circuit elements.

F) Create a project directory and a cds.lib file (for every project)

The best way to organize work is to use multiple directories with each directory being dedicated to a specific class or to a research project. I created a new directory where all of the libraries will be stored for this course. Next, I typed the following command into the terminal to create the ee330 folder: mkdir ee330

I then changed into the new directory using the "cd ee330"command. I copied several files by typing the following commands at the prompt.

cp /remote/ncsu_oa/local/cdssetup/cdsenv ~/ee330/.cdsenv
cp /remote/ncsu_oa/local/cdssetup/cdsinit ~/ee330/.cdsinit
cp /remote/ncsu_oa/local/cdssetup/cds.lib ~/ee330/ cds.lib
cp /remote/ncsu_oa/local/cdssetup/display.drf ~/ee330/display.drf
I then opened my ~/ee330/cds.lib file and added the following line to its contents:
INCLUDE ~/cds.lib

This line includes the contents of the ~/cds.lib file giving access to the common libraries defined there. The file will be automatically updated whenever I launch Cadence IC tools from ~/ee330. Finally, I edited the ~/ee330/.cdsenv file. Using a text editor, I added the given lines of code (given in lab handout) under their respective heading to the .cdsenv file. The basic setup for running the Cadence Custom IC design tools is now complete. I then logged off the computer and logged on again.

2. Starting Cadence Custom IC tool and creating libraries

To begin this step, I typed the command "bash" into the terminal. I continued into the ee330 directory and typed the command: virtuoso &. This opened up Cadence, the Command Interpreter Window (CIW), and Library Manager. The CIW will become very helpful when troubleshooting. The library manager organizes the data into various libraries and cells. Below is an image of my library manager.

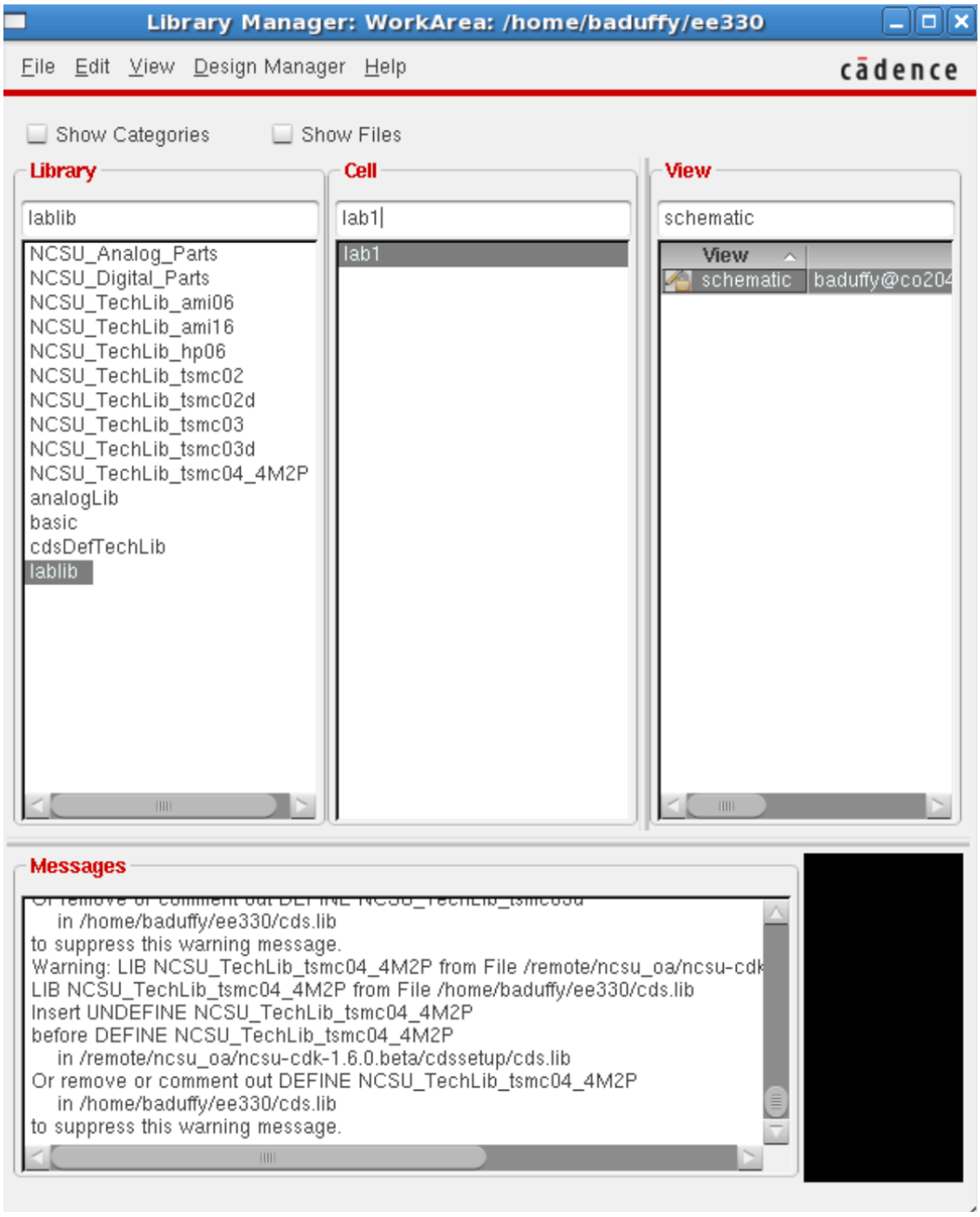

Figure 2: Library manager

A) Creating a new library

During this lab, all designs will be grouped in Libraries. Each library is looked at as folder grouping related sub-folders in one location. Each library can have many cells with multiple

views. The first step was to create a new library, "lablib", and create cells for each lab in the library. I did this by clicking **File→New→Library**. This new library then opened in the library manager.

B) Creating a new cell and a cell view

This next step was to create a new cell and cell view. A cell in Cadence can represent any level of hierarchy of a design. Each cell has at least one "cell view." A cell can have a behavioral view, a schematic view, and a symbol view, etc. In order to make a new cell, I clicked on **File→New→Cell View...**in the Library manager. I created a view cell called lab1 with schematic view in the lablib library. After that, the program was now ready to begin circuit simulation.

3. Schematic Capture

I then took the following steps to insert the low pass filter circuit in Figure 1 into the schematic. The first step is to instantiate all the required components.

A) Instantiating the components

Create→Instance is a way to place components in the schematic. In the "Component Browser", I changed the library to "analogLib" and clicked on "Flatten" to see all the cells without categorization. Adding the resistor, "res" to the schematic was then simple and easy to figure out. Once I included the resistors, I instantiated a capacitor (cap), ground (gnd), and a voltage source (vsource) from analogLib.

B) Connecting the components

One way to interconnect components is by using the menu entry **Create→Wire (narrow)** and click on the red terminal of a component to start one end of the wire and end by clicking on the other component's terminal. The second option is to bring the mouse pointer over the red terminal over the first component's terminal and then click and drag the mouse until the completion of your connection to another component. The "check and save" feature is another aspect to the design that is important use. This makes sure there are no floating components or connection issues.

C) Adding labels

As components are wired together, every net is automatically assigned a name such as net1, net2, etc. These names are difficult to remember, so adding labels to wires helps to become more efficient. To do so, I clicked on **Create→Wire Name** typed **vIn vMid vOut** and clicked on the respective wire to do the labeling.

D) Editing object properties

If mistakes need corrected, clicking on the object and then clicking **Edit→Properties→Objects** can make the changes**.** Now the simulations are ready. For

those simulations to work, I provided appropriate input stimuli.

– For DC simulation, in the "DC voltage" box, I made the input for the dc analysis to be one.

– For AV analysis input, I turned the option to on in "Display small signal params." I made the input value in the AC magnitude" to be 1V.

– For transient analysis, I chose the "Source type" field to the type needed. I then entered all the applicable entries and clicked on OK.

The vsource component is now configured for simulations. I was sure to click "Check and save" to save my design.

E) Adding comments

In order to add comments for good practice, I clicked on **Create→Note→Text** to include a useful reminder about the schematic. You can view the finalized schematic below in Figure 3.

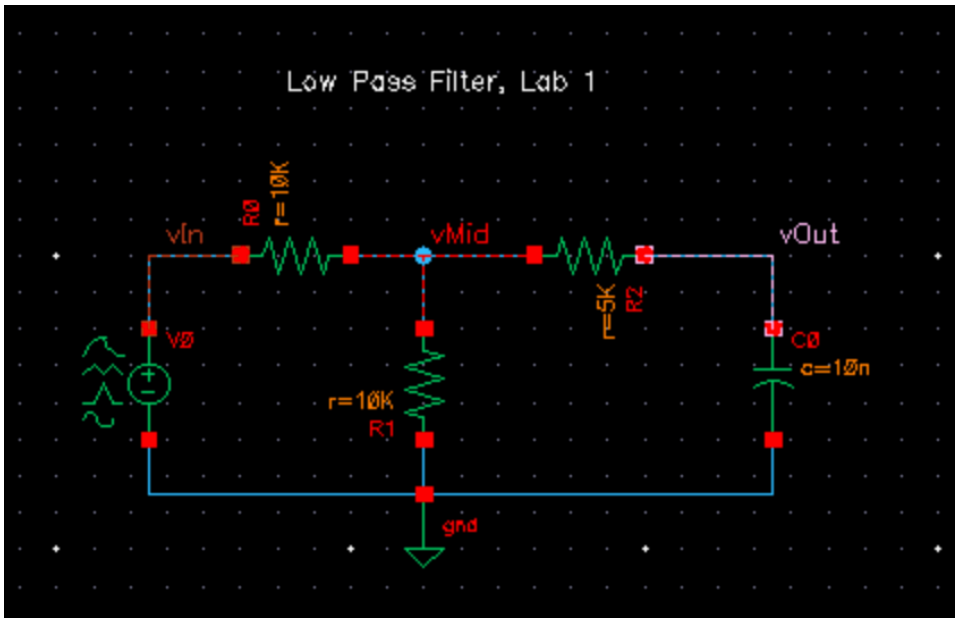

Figure 3: Low-pass Filter Schematic

4. Simulating a circuit

Once the schematic capture was complete, I simulated the circuit to test if it performs according to the design. To do this, I opened the Analog Design Environment (ADE) window by taking the following steps:

Launch→ADE L

After opening the ADE window, I clicked

Setup → Simulator/Directory/Host

and set the Project Directory path to

/local/baduffy/ cadence/simulation

Doing this causes the simulation data to be stored on the /local/ rather than in my account space. The ADE window is then used to select a simulator as well as set up all the options and simulations for the simulator.

A) Setting up the simulations

I began using ADE by discovering the various task icons on the right side of the window. I then clicked on the **Choose analyses...** icon to bring up the "Choosing Analysis" form. The dc analysis was my first analysis. In order to do this, I clicked on the dc button, which popped up the form contents showing entries relevant to a dc analysis. I chose my sweeping input voltage from 0 to 5 volts. To sweep the input dc voltage, in the "sweep variable" box area I clicked on the "component parameter" button.

To select the dc input voltage of the vsource, I clicked on "Select component" and then vsource in the schematics window. In the new form that pops up, I chose dc to make vsource have a dc voltage. Next, I entered the range of the sweep in the start and stop boxes (0 to 5). After clicking "apply," changes were in effect.

B) Setting up the outputs

To tell the simulator which node voltages I need to be plotted, I clicked on the menu item **Outputs→To be Plotted →Select on Schematics.** Then I clicked on the three labels added earlier to select those voltages to be plotted.

C) Running the simulation and viewing the results

Now that I set up which type of analysis to run and which outputs to produce, I clicked on the green arrow to start simulation. Results can be viewed below.

Results and Analysis

DC Analysis

The DC analysis proved to yield correct results from the pre-lab. From pre-lab question 3, Vin= ½ Vmid and Vmid=Vout. Capacitors act as a break in the circuit when DC voltage is applied to them. Therefore, the voltages are exponentially increasing. This can also be seen below.

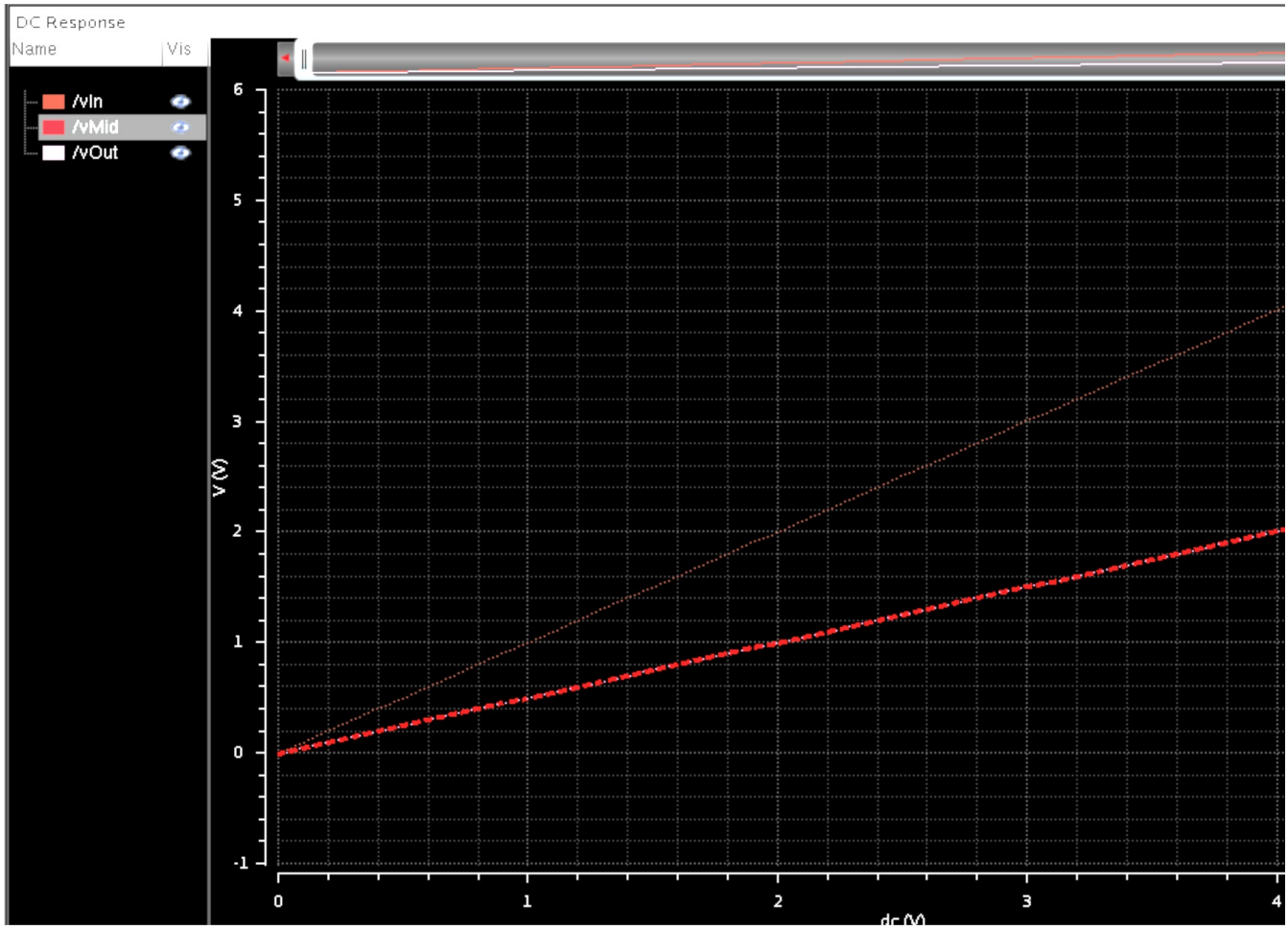

Figure 4: DC Response

AC Analysis

In the AC Analysis found below, the -3dB corner frequency is verified by the pre-lab. I found the answer to this low-pass circuit to have a -3dB corner frequency of 1591.55 Hz, which can be found from 1 Hz-3kHz. You can see below that I found the corner frequency of Vout to be very close to this value.

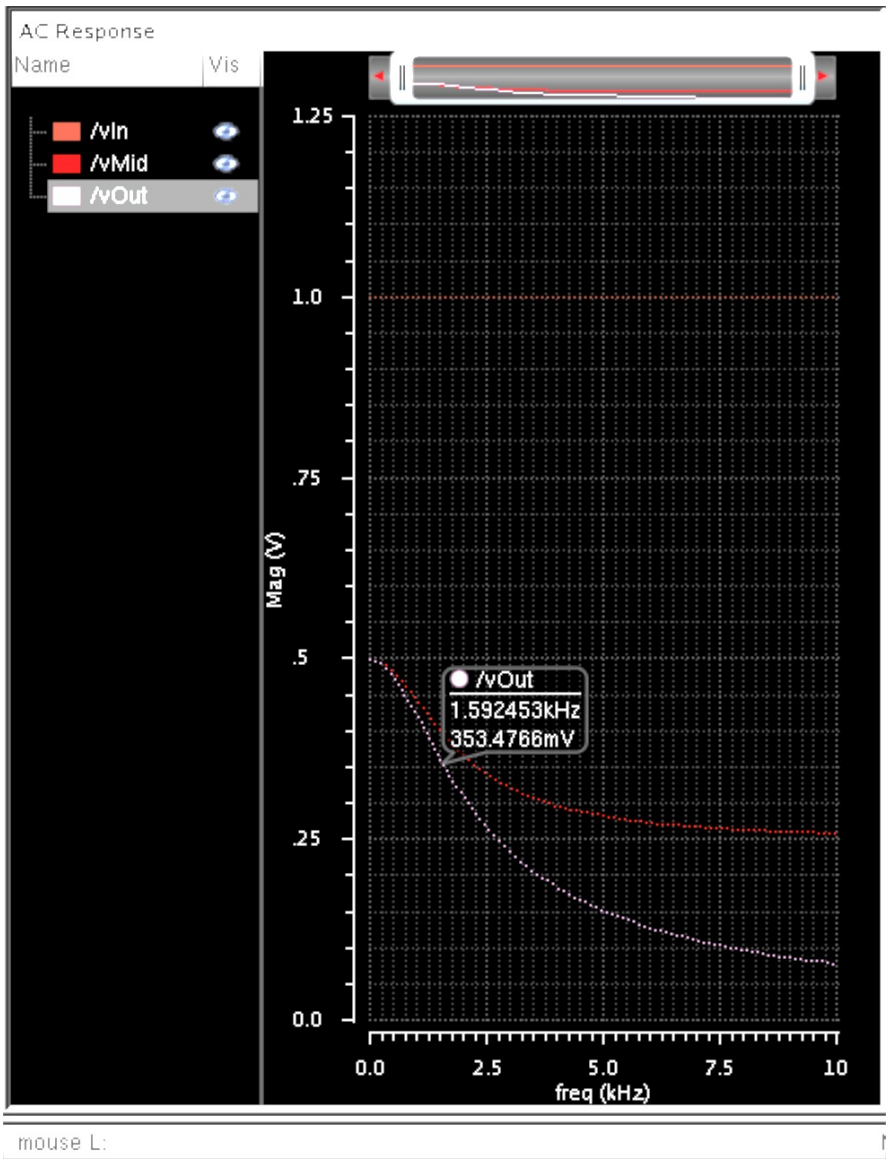

Figure 5: AC Response

Transient Analysis

The transient response is the response of a system to a change from equilibrium. During this analysis, you will see the rise and fall time. In general, a capacitor takes 5 time constants to fully charge and 5 time constants to discharge. Due to this knowledge, I set the time length to .001 seconds to run the transient analysis in order to view all the information.

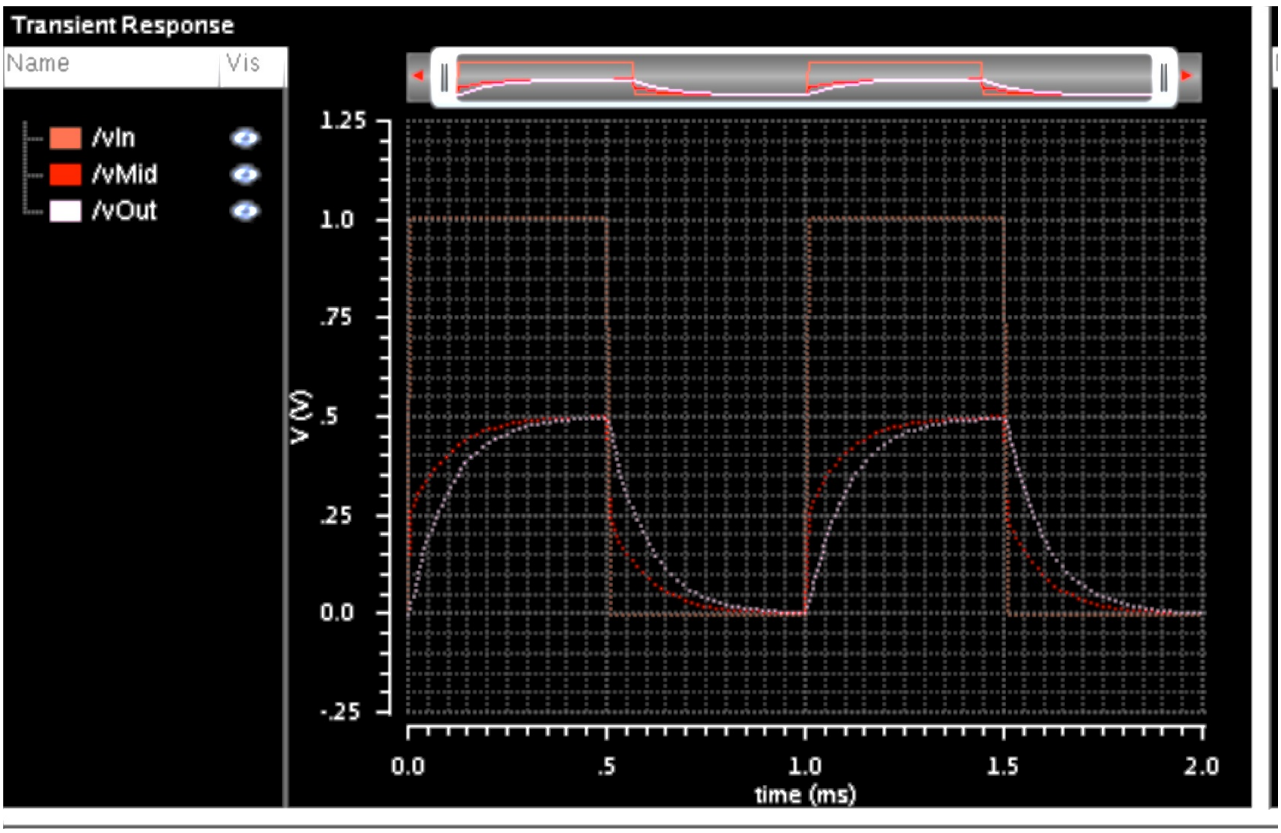

Figure 6: Transient Response

Conclusion

During this laboratory, I was able to review many EE 230 topics. I was really able to familiarize myself with the Cadence Virtuoso software, the schematics editor, and simulation of the circuit using ADE. In addition, I gained a better understanding of the difference between a CAD software program and SPECTRE.