Lab 3: Layout and LVS
(Layout vs. Schematic)

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Introduction

The goal of this lab was to introduce the concept of circuit design layouts. In this context, design rules and CAD tools were used in this lab to verify that all design rules were satisfied. This is done by design rule checkers (DRC). The final objective was to verify the actual equivalent circuit corresponding to the layout agreed with the original circuit schematic. A CAD tool that performs this latter function, termed a layout versus schematic (LVS) tool will be used for this purpose. The lab report will provide details about the experiment, observations, and results I found along the way.

Procedure and Results

Part 1: Layout View

First, we were introduced to layout view in the design environment of Cadence Virtuoso. A layout view gives us a good representation of what the semiconductor circuit looks like after fabrication. Once all design rules are passed, found free of violations, and electrically equivalent to the schematic, it is sent to the foundry for fabrication.

I created the layout of the inverter created in lab 2. In the process of designing this layout, I discovered many features including: the toolbox entitled *Layers*, grid settings, creating shapes, rulers, stretching shapes, creating contacts, creating pins, and much more. Below, you can see the layout of the inverter in Figure 1.

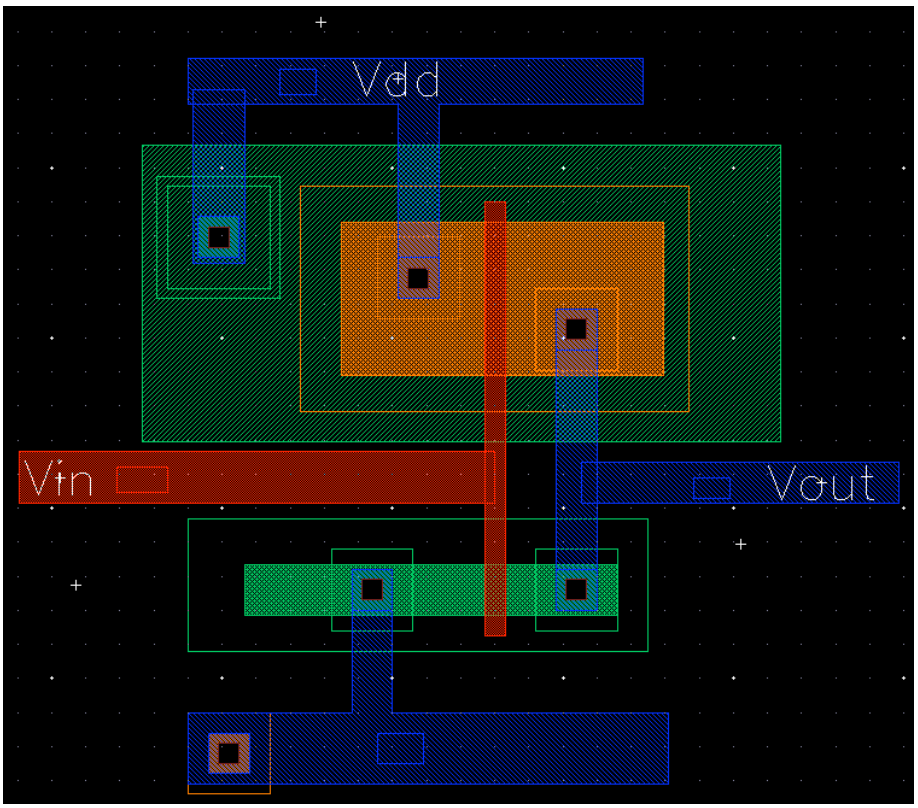

Figure 1: Layout of Inverter (Vss not shown, but is there)

Part 2: Checking for errors

After finishing the layout, the next step was to check for errors in the layout. To check the layout, I went to Verify→ DRC→ OK. With this, the Design Rule Check will check the layout for any inconsistencies or errors and report back. The first time I ran DRC, I had many minor errors. In order to debug my errors, I went to Verify → Markers → Explain, and clicked on the white error markers on my layout. Guessing what the white marks mean was fairly simple to figure out. After moving a variety of shapes around, finally my CIW window showed zero errors (Total errors found: 0)—this means that my layout was free of errors, ready for any simulation, meets all benchmarks, etc. Please see Figure 2 below.

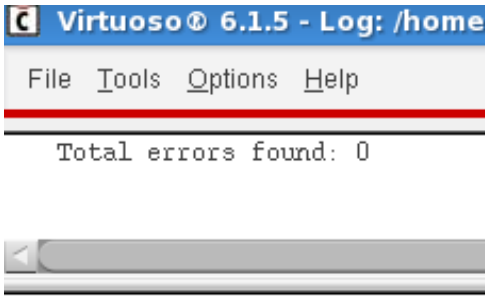

Figure 2: CIW window showing zero errors

Part 2.1: Layout vs. Schematic (LVS) comparison

Once the layout was finalized, the next important step was to check for consistency with the schematic it is supposed to represent. The comparison ensures that there are the same number of devices, and also that they have the same I/O pins and device sizes. The extraction of the layout was done next. This takes the layers of semiconductor material (layout) and goes to an identification of the various components such as their sizes and pins (extracted.) In order to do this, I clicked Verify → Extract → OK. The extracted image can be seen in Figure 3.

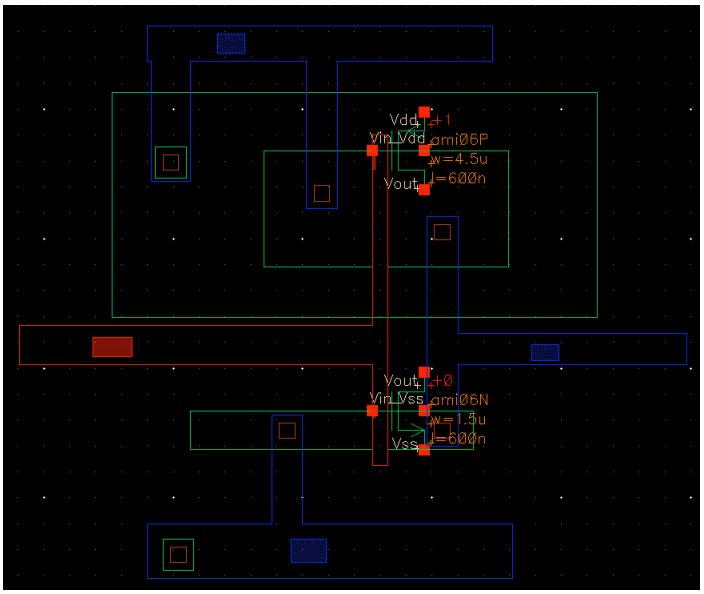

Figure 3: Extracted inverter layout

The next step was to run the LVS by clicking in either the layout or extracted image and going to Verify → LVS. I made sure I was comparing the right schematic and extracted views by hitting Browse. The first time I hit Run, I had an error message. After trying various ways to fix the situation, I had no luck. I then received help from a TA who could also not figure out the issue. After an hour of trying to discover the problem, we tried unchecking the "Correspondence File" like you see in Figure 4. This solved the issue. This "Correspondence File" has certain parameters that were not needed during this lab.

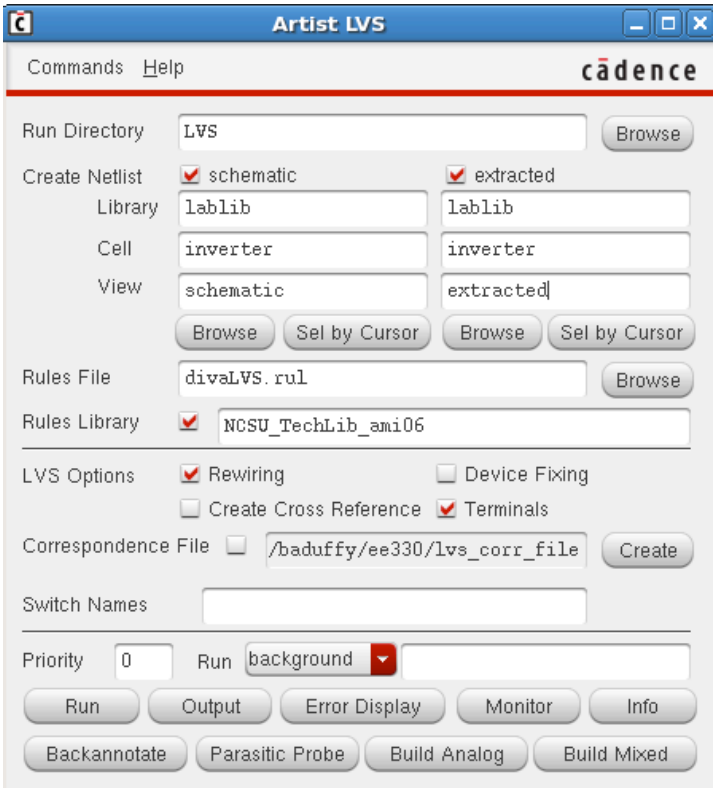

Figure 4: LVS features

Once the LVS was verified, I received an output log seen in Figure 5 on the next page.

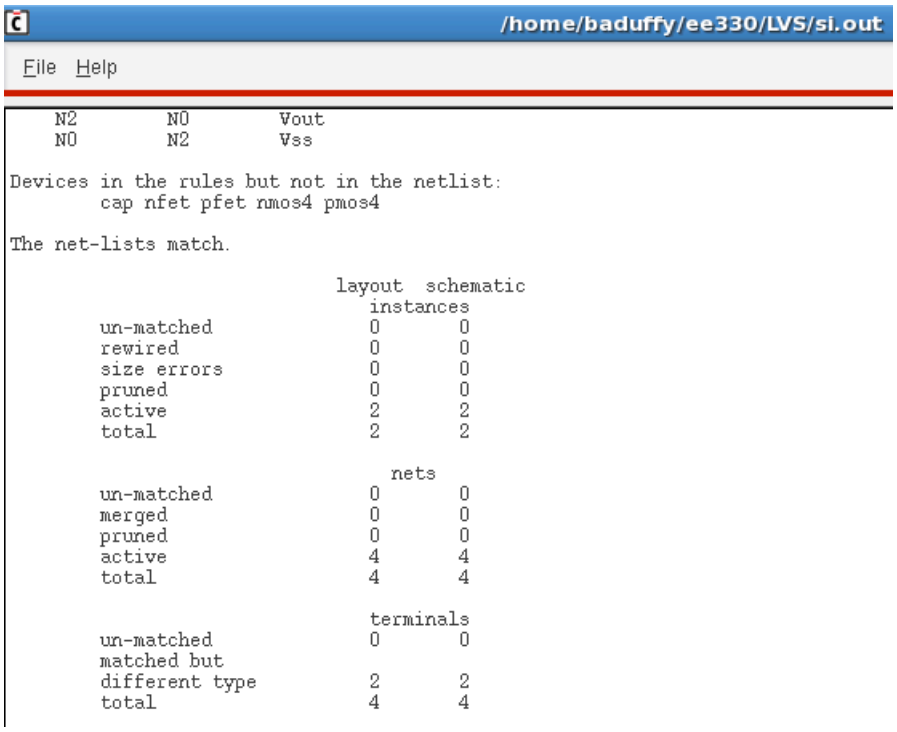

Figure 5: Output Log of si.out

As seen in Figure 5, the "net-lists match." This indicates that everything was correct and matches in the schematic and layout.

Part 2.2 How to locate a net on the extracted view

In order to make it easier to find an extracted view, probing the design makes it easier to do. I chose Verify/Probe. In the Probing form, I clicked on Add Net. I then went to the CIW and typed "X" at the command prompt and pressed Enter. A mask layer being highlighted then appeared with the given net name.

Conclusion

From this lab, I learned a great deal about what effort is put into drawing a layout of a circuit with CAD tools. After this process was finalized with many trial and errors, I have a better understanding about the design rules and the importance of sizing according to specifications. Another aspect of Cadence I learned was how to verify the layout agrees with the original circuit schematic using the LVS tool. As I look towards the future, I believe this lab will truly help my understanding of VLSI. As I progress through this course, I see an increasing trend of the importance of verifications of workflow in order to assure good product output.